Invited Paper:

Toward Energy-Efficient High-Performance Organizations of the Memory Hierarchy in Chip-Multiprocessor Architectures

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ABSTRACT

Chip-multiprocessor systems or CMPs have emerged as a high-performance organization for the increasing number of transistors available on a chip, and are projected to dominate the market of server and desktop computers. CMPs require innovative designs of on-chip memory hierarchies, especially designed to address the problems that arise in this novel kind of architecture: higher memory bandwidth demand from more processing cores and the increasing latency of off-chip cache misses. Moreover, the energy consumption topic is even more pressing than in traditional multiprocessors, as the CMPs are commonly used in embedded systems. This paper presents a survey of some of the proposals that have recently appeared facing these topics.

Keywords: Chip-multiprocessors, Memory Hierarchy Organization, Cache Miss Latency, Cache Storage Use, Energy-Aware Techniques

1 INTRODUCTION

As integration scales grows, the number of transistors available on a die is increasingly becoming larger, and billion transistor chips are possible nowadays [6]. The role of computer designers is to translate all this raw potential into increased computational power. For this, efficient architectures must be designed. One of the approaches recently proposed in the literature to make efficient use of this huge number of transistors is single chip-multiprocessors [3, 10]. A CMP integrates several processor cores onto a chip, as well as other resources such as the cache hierarchy and the interconnection network. As a result, the traditional advantages of parallel architectures are kept, but some of their drawbacks, such as wire delays or network latencies, are minimized.

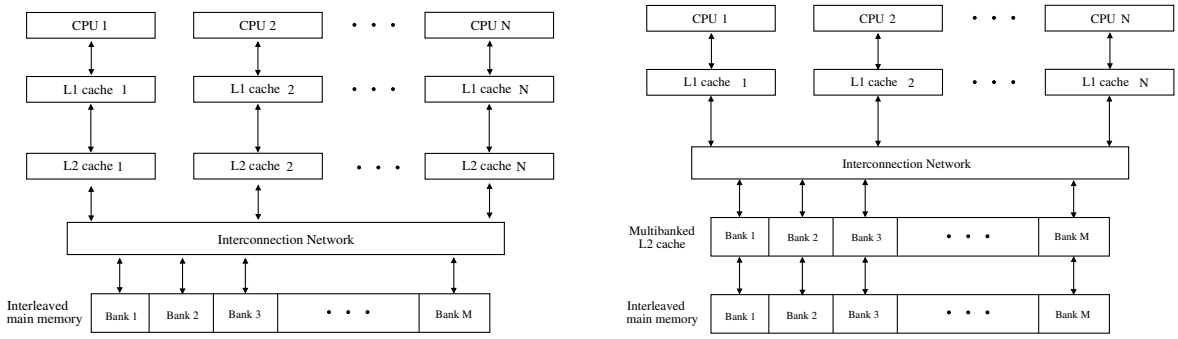
The viability and importance of chip multiprocessors is further supported by a number of recently announced commercial CMP designs [16, 21, 22]. However, nowadays the best organization of the components in this kind of architecture has not been defined, and there is still much work to be done in order to improve the performance and maximize the utilization of the resources in a CMP.

One of the topics that more efforts is deserving by the researchers is the organization of the cache hierarchy [11, 31]. The combination of the high bandwidth demands from the processing cores, together with the high cost of cache misses, makes this issue especially critical for future chip-multiprocessors.

There are two major alternatives for organizing the last level of the cache hierarchy in a CMP [29] (from now on, we suppose that the L2 cache is the last level of on-chip cache): *private* or *shared* L2 cache (see Figure 1). In the private L2 cache organization (Figure 1(a)), the total cache storage is partitioned between the processor cores, and misses from the L1 cache go directly to the private L2 cache without crossing the shared interconnection network. In the shared L2 cache organization (Figure 1(b)), the L2 cache storage is shared by all the processors and cache coherence is maintained at the L1 cache level.

Each approach has different pros and cons. In the private cache organization, most of the L1 cache misses can be handled by the L2 cache, so the number of remote on-chip L2 cache accesses is reduced and it is not necessary to cross the interconnection network, which reduces the miss latency. However, private L2 caches make inefficient use of the total cache storage space, as multiple copies of the same line can reside in different private L2 caches. Another issue regarding the private L2 cache organization is the load balance problem that can arise due to the static assignment of L2 cache space to processor cores.

On the other hand, a shared L2 cache organization can reduce the collective number of L2 misses, as there are not replicated copies of the same line. Besides, the load balancing problem can be solved with a nonuniform distribution of the cache space between the cores. The main drawbacks of this organization are the higher hit latency, as the interconnection network must be used to access remote L2 cache banks, and the possible interference between cores, as each one can evict the blocks that other is using.



(a) Private L2 cache.

(b) Shared L2 cache.

Figure 1. Private vs. shared L2 cache organizations.

Several proposals have recently appeared in the literature that attempt to achieve the benefits of both basic organizations. As we can see, the design of the cache hierarchy in a CMP is a very complex problem in which all the variables previously mentioned must be taken into account.

Another interesting topic to keep in mind when designing a CMP architecture is the thermal/energy consumption. As processors continue to increase in speed, energy consumption and heat dissipation have become key design variables, especially if we take into account that chip-multiprocessors architectures are suited for the embedded computing domain, where the energy consumption restrictions are more pronounced. Increased power consumption and heat dissipation typically leads to higher costs for thermal packaging, fans, electricity, and even air conditioning, so it is imperative to design energy-aware chip-multiprocessor systems.

In this paper, we present a revision of the alternatives that have been recently proposed addressing these two important issues in CMP architectures: cache hierarchy organization and energy consumption. First, in Section 2 we depict several proposals aimed at reducing the cache miss latency. In Section 3 we describe some cache organizations aimed at optimizing the use of cache storage. Then, in Section 4, some techniques facing the power consumption problem are presented. Finally, Section 5 concludes the paper.

2 REDUCING CACHE MISS LATENCY

As we have stated in Section 1, private L2 cache organizations suffer from lower L1 cache miss latencies than shared L2 cache architectures at the expense of poor cache storage utilization. In this section, we describe some proposals aimed at approximating the latencies of private caches while maintaining the advantages of shared organizations.

Several authors propose a hybrid cache scheme which tries to retain the advantages of a shared L2 cache but minimizing the miss latency. In [37], the authors present a new cache management policy called *victim replication*. In their proposal, the L2 cache space is divided into several slices which can be managed as private or shared. The basis of this mechanism consists in allowing multiple copies of a cache line in different slices. In this way, each processor has a dynamically formed private L2 cache.

In Nonuniform Cache Access (NUCA) designs, the problem of on-chip wire delays is addressed. This problem makes large shared L2 caches with an unique hit latency a bad design choice [1]. Several on-chip cache designs exploiting the NUCA concept are evaluated in [18, 19]. The S-NUCA-1 design features a two-level cache hierarchy in which the inclusion property is not maintained. The mapping of data into banks is performed statically and each bank uses a pipelined transmission channel to service requests. S-NUCA-2 improves the previous design by using a two-dimensional switched network, as the area requirements of using a dedicated transmission channel becomes prohibitive when the number of L2 cache banks increases. A third design named D-NUCA includes a mechanism of block promotion in order to exploit the lower hit latency of nearer cache banks. In this architecture, blocks are migrated to faster banks (the nearest banks to the consumer) in order to reduce L2 hit latency.

The D-NUCA concept is applied to CMP architectures in [12], where the authors evaluate different sharing degrees in order to find the optimum compromise between cache space utilization and hit latency. Two migration policies are investigated: D-NUCA 1D, which allows migration only in the vertical dimension, and D-NUCA

2D, in which migration can happen in the horizontal dimension as well. In order to prevent the situation in which a block is migrated from one cache bank to another because two processors are accessing it, the authors propose a two-bit saturating counter which allows the migration only if the counter corresponding to that direction is saturated.

The proposals contained in [34] refer to a hybrid CMP/SMT architecture with two levels of private cache and a third level of on-chip shared cache. As the L2 cache access latency is much lower than the L3 cache one, they consider the case in which write backs from an L2 cache can be placed in a neighbouring cache instead of the further L3 cache. They use a small table to keep track of those lines with a high reuse potential. This table annotates the lines that were written back and later reused by another L2 cache.

In [4] the authors evaluate three well-known uniprocessors techniques for reducing L2 cache latency. The first technique is hardware-directed strided prefetching [14]. They use L1 and L2 prefetching and find that this technique can hide L2 cache latency in great extent. The second technique evaluated is the D-NUCA block migration policy previously commented. They observe that without an intelligent block migration algorithm, as the one proposed in [12], shared blocks tend to migrate to the central cache banks, which are equally distant from all the processors. Finally, transmission line caches (in which on-chip transmission lines are used in order to provide low access latency to all the banks) are evaluated; the technique exhibits similar results to those found in uniprocessor architectures, but the contention in the dedicated lines becomes an important fraction of the overall L2 hit latency. The authors evaluate a hybrid scheme which combines the three techniques and propose using transmission lines only to access the central banks where the cache lines are concentrated due to block migration.

Another proposal related to the on-chip communication mechanisms can be found in [5]. In this paper, the authors optimize the producer-consumer coherence pattern, in which the copy of the line in the reader cache is invalidated on every write and subsequently read again. They propose an implementation in which a single copy of the block is maintained for the lines that exhibit this behavior. In their implementation, the copy is stored close to the reader, as they observe that in their evaluation environment (composed of commercial workloads) each write is read more than once by each reader. They add a communication state to the coherence protocol in which the writer can write the block and the readers can read it without incurring in a coherence miss.

Synchronization using a shared variable is a well-known problem in shared-memory multiprocessors [24]. This problem is addressed in the context of a multiprocessor-on-a-chip in [36]. The authors propose a mechanism named *Tagged Shared Variable Memory* (TSVM) which stores the shared variables used in synchronization in a dedicated cache. The TSVM is divided into two structures: the TSVM cache (TC), which works as a L1 cache for synchronization variables, and a conventional memory. Thus, the L1 cache can be viewed as a memory with a dedicated portion for synchronization variables (the TC) and a *General Variable Cache* (GVC) that caches the remaining variables. As the hit latency for synchronization operations is reduced, the performance of the applications evaluated is boosted notably.

3 OPTIMIZING THE USE OF CACHE STORAGE

While the proposals described in the previous section are aimed at reducing the cache access latency, some recently proposed mechanisms try to optimize the use of cache capacity.

Liu *et al.* investigate different organizations for the L2 cache in [29], addressing the tradeoffs between private and shared L2 cache organizations. They propose a hybrid organization for the L2 cache called *Shared-Processor Based Split*. In this organization, accesses to the cache are based on the CPU cores rather than on the memory address (as in typical shared L2 caches), which allows better balance of the load between processors. The total L2 cache space is divided into several chunks which are assigned dynamically to the processors. In this way, the Shared-Processor Based Split L2 cache provides a flexible way of configuring the L2 cache based on workload characteristics.

Block replication is the basis for some of the proposals contained in [5]. In order to prevent the waste of on-chip capacity caused by uncontrolled replication, they avoid this replication when a copy of the shared line exists in the private cache of another processor. As the copy is on-chip, the latency penalty is small and it does not overcome the benefits of the improved use of cache storage. Another mechanism proposed in the same paper controls the case in which a core needs more capacity than the provided by its private cache. With the *capacity stealing* technique, the less-frequently-used blocks of the core which needs more cache capacity can be placed in the caches of the closer cores with less capacity demands. This strategy reduces the higher miss rates typical in private cache organizations.

The authors of [34] propose a small history table in order to perform smart write backs in the context of a three-level cache hierarchy with two levels of private cache. On a replacement of a clean line, the cache controller consults this table in order to know if there is another copy of the line in an L2 cache or in the L3 cache, so that it is possible to make a more informed decision about writting back the line or not. This table is associated with each L2 cache in the system and is organized as a cache tag array.

Iyer proposed in [13] a priority-based cache management mechanism to allocate cache resources by priority. The paper discusses several options for priority classification, assignment and enforcement, placing special emphasis on the last topic. To enforce priorities in the framework, three possible schemes are discussed: static/dynamic partitioning (higher priority applications have more ways in cache sets than lower priority ones), selective cache allocation (allow/disallow allocation based on the current cache space used and the priority given to each kind of traffic) and heterogeneous cache regions (where heterogeneous cache structures with different set associative, for example, are mapped to memory access streams with different priorities).

Settle *et al.* study the effects of thread interference in *simultaneous multithreading* CMP architectures [33]. Interference occurs in the cache system when data belonging to one thread is evicted by a cache line from another thread. To solve this problem, they also use cache partition techniques, and the space assigned to each thread is reassigned dynamically based on the degree of global data reuse of lines previously evicted and the percentage of cache storage already allocated to the thread. In this way, threads that exhibit low reuse due to the lack of cache storage can compete with threads showing high reuse because they own most of the lines.

Another work related to CMP/SMT architectures is [35]. This work presents a cache partitioning scheme that dynamically allocates cache space using a set of counters. These counters are used to estimate the changes in process miss rate when allocating/deallocating cache storage to that processor. The replacement unit keeps track of the number of cache blocks belong to each active process, and allocates a new cache block to a process only if its current allocation is below its limit.

Kim *et al.* presents a detailed study of fairness in cache sharing between threads in [20], where fairness measures how the threads are slowed down due to cache sharing. They propose five cache fairness metrics and static/dynamic cache partitioning algorithms which use these metrics. The dynamic algorithm does not restrict the cache replacement algorithm to LRU, as some of the proposals described previously require. Finally, the paper correlates fairness and throughput and shows that optimizing fairness usually increases throughput.

4 ENERGY-AWARE TECHNIQUES IN CMPS

While the proposals summarized in the previous sections are aimed at improving the performance of the memory subsystem in chip-multiprocessors, another important topic regarding this kind of architecture is the energy consumption, as we have discussed in Section 1. This section covers this issue and describes some energy-aware proposals.

Some of these proposals are based on the dynamic voltage/frequency scaling. A first work by Li and Martínez [27] develops an analytical model in which the variables are efficiency, application granularity and voltage/frequency scale. The work shows that tuning the levels of voltage/frequency correctly, great energy savings can be obtained. However, the choice is dependent on the application and the process technology, which complicates this voltage/frequency scaling.

The previous work is extended in [26], where the authors propose a mechanism which optimizes dynamically the energy consumption of a parallel application running on a CMP composed of 16 processor cores under certain performance restrictions. They present a set of heuristics applied to the number of active processor cores and the dynamic voltage/frequency scaling, which are typically the two most important dimensions of the energy-aware design space.

The proposal contained in [15] follows a compiler-based approach. The compiler takes advantage of the heterogeneous parallel execution of the workloads in different processors and assigns different voltage/frequency pairs to different processors if the energy consumption is reduced and, at the same time, the increasing of the execution time is not significant.

Another approach followed in some works to reduce the energy waste relies on the use of heterogeneous multi-core architectures. In [23] several single-ISA heterogeneous multi-core designs are proposed and evaluated in the context of multiprogrammed workloads. The different cores represent some points in the performance/energy design space; during the execution of an application, the system software chooses dynamically the more appropriate core in order to meet with the specific requirements of energy and performance of the application.

The goal pursued in [2] is minimizing the execution time of multithreaded programs containing parallel and sequential phases in their execution, while maintaining the energy consumption within a limited interval. In this case, the *Energy per Instruction* (EPI) parameter of the formula $Power = EPI * InstructionsPerSecond(IPS)$ is modified according to the amount of available parallelism in an asymmetric multiprocessor with four cores.

Another evaluation of a CMP environment limited by the energy can be found in [9], where the authors evaluate the compromise between latency performance and throughput performance. Their proposal is also based on varying the amount of energy wasted to process the instructions taking into account the level of parallelism available in the software. To accomplish this, they use a combination of well-known energy-aware techniques: voltage/frequency scaling, asymmetric cores, heterogeneous cores and speculation control.

The problem of thread synchronization using barriers is addressed in [30]. By using a high-level synchronization constructor, the proposed technique tracks the idle intervals in which a processor is waiting for the other processors to reach the same point in the program. Using this information, the technique modules the frequency of the different processors in order to remove the idle intervals and then reducing the energy consumption.

The compromise between the issue width of processor cores and the number of cores on a chip is analyzed in [8]. All the designs evaluated feature comparable sizes and the comparison is performed with respect to both performance and energy waste. The results show that it is possible to achieve the same performance with narrower cores and with lower energy consumption.

A recent work [28] shows that the thermal restrictions dominates over other physical restrictions in CMP architectures. As an important conclusion, for aggressive cooling solutions reducing power density is at least as important as reducing total power, while for low-cost cooling solutions they suggest that reducing total power is more important.

Finally, there are a couple of works dealing with CMP/SMT implementations and the energy efficiency of these two families of architectures. A work measuring the potential for techniques aimed at reducing the energy consumption in these architectures appears in [7], where the authors find that both architectures present prominent temperature gradients but, at the same time, they show a great potential for temperature-aware enhancements to mitigate the problem.

Kaxiras *et al.* evaluate the power consumption of a SMT and a CMP DSP for mobile phone workloads [17]. They find that the SMT VLIW DSP uses up to 40% less power than the CMP DSP in their target environment. The results are different in an environment composed of out-of-order processor cores, like the one evaluated in [32]. In this case, the results show that the CMP alternative is more efficient in terms of energy consumption but requires more area to be implemented, so the authors propose a hybrid architecture where a CMP integrates several SMT cores. Taking the number of pipeline stages and the pipeline width as metrics of the core complexity, Lee and Brooks evaluate the energy/performance tradeoff of several SMT and CMP architectures of varying complexity [25]. Their results suggest that SMT architectures enable efficient increases in pipeline dimensions and core complexity, while reducing pipeline dimensions in CMP cores is inefficient.

5 CONCLUSIONS

Chip-multiprocessor systems or CMPs have emerged as a high-performance organization for the increasing number of transistors available on a chip, and are projected to dominate the market of server and desktop computers. However, the best organization of the components in this kind of architecture has not been defined yet, and there is still much work to be done in order to improve the performance and maximize the utilization of the resources in a CMP.

This paper surveys some of the proposals that have recently appeared focusing on two of the more critical issues when designing a CMP architecture: the organization of the cache hierarchy and the use of techniques aimed at reducing the energy consumption. In the organization of the cache hierarchy we have shown possible ways of reducing the latency of the cache misses and a couple of proposals that attempts to improve the use of the cache storage. Regarding the energy consumption, several works show the potential of future energy-aware techniques applied to CMPs and some optimizations in the domains of voltage/frequency scaling, thread synchronization, heterogeneous multi-core architectures, issue width and hybrid CMP/SMT architectures have been described.

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